REMARKS

The forgoing Amendment and remarks which follow are responsive to the Office Action mailed November 19, 2003 in relation to the above-identified patent application. In that Office Action, the Examiner rejected Claims 1-6, 9-11 and 19-25 under 35 U.S.C. §103(a) as being obvious over the combination of the Huang et al and Abe references. Additionally, the Examiner rejected Claims 7 and 8 under 35 U.S.C. §103(a) as being obvious over the combination of the Huang et al, Abe and Song references.

Summary of Claim Amendments

By this Amendment, Applicant has cancelled Claims 10 and 25. Additionally, Applicant has amended independent Claim 1 to include the limitation originally recited in cancelled Claim 10, and has amended independent Claim 19 to include the limitation originally recited in Claim 25. As such, Claims 1 and 19 as amended each describe the first semiconductor die and the leads as being oriented relative to each other such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact any of the leads.

Amended Independent Claims 1 and 19 are not Rendered Obvious by the Combination of the Huang et al and Abe References

Independent Claim 1 as amended recites, inter alia, "*...po rtions of the first surface of the first semiconductor die being directly attached to the second surface of each of the leads, the first semiconductor die and the leads being oriented relative to each other such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact the second surface of any one of the leads...*".

Independent Claim 19 as amended recites, inter alia, "*...the first semiconductor die being directly attached to each of the leads, the first semiconductor die and the leads being oriented relative to each other such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact any of the leads...*".

Applicant respectfully submits that the combined teachings of the Huang et al and Abe references clearly do not teach, suggest or show any embodiment of a semiconductor package having the above-described structural attributes as recited in each of Claims 1 and 19 as amended.

In the embodiment of the semiconductor package shown in Figure 7 of the Huang et al reference (relied upon by the Examiner), a first or lower chip 304 is shown as being mounted to the top surface of the die pad 318 via a layer of adhesive 322. Disposed about the periphery of the die pad 318 are a plurality of leads 326, each of which includes a first or top surface 328a, and a second or bottom surface 328b which has a stepped structure defining a protruded zone 330. Stacked upon the lower first chip 304 is an upper second chip 310 which is secured to the first chip 304 by a layer of adhesive 324. As clearly shown in Figure 7, no portion of the lower surface of the chip 304 is attached to top, first surfaces 328a of the leads 326. Rather, the leads 326 are disposed well outward of the peripheral edges of the first and second chips 304, 310. The deficiencies of Figure 7 of the Huang et al reference hold true for the single chip embodiments shown in Figures 3, 5 and 6 thereof.

The Abe reference discloses a semiconductor device 1 having a leadframe 10 and a semiconductor element 14 which is mounted to the leadframe 10 through the use of an adhesive tape 12. The semiconductor element 14 is electrically connected to the leadframe 10 through the use of bonding wires 16 which, along with the semiconductor element 14, are sealed or encapsulated with a resin material 18. The leadframe 10 of the semiconductor device 1 in the Abe reference includes a plurality of terminal portions 10a which protrude through the substrate mount surface of the resin material 18 and each have a solder layer 19 applied thereto. As is specifically stated in the specification of the Abe reference, the application of the solder layer 19 to each of the

terminal portions 10a made possible by the protrusion of the terminal portions 10a through the substrate mount surface of the resin material 18 allows the terminal portions 10a to be used as connecting terminals, thereby eliminating the need for solder balls for mounting as required in conventional ball-grid array semiconductor devices and thus providing substantially reduced material and manufacturing costs (see Abe specification, column 3, lines 46-58).

In the Office Action, the Examiner states that it would have been obvious to one of ordinary skill in the art to modify the semiconductor device of Huang et al to include portions of the die attached to the leads as disclosed in Abe because it aids in reducing manufacturing cost. In support of this argument, the Examiner makes reference to the passage of the specification of the Abe reference beginning in column 1, line 50 and ending in column 2, line 19. However, this language simply mirrors that described above in column 3, lines 46-58 of the Abe reference. In this regard, both the language of this passage and that cited by the Examiner demonstrates that the reduction in manufacturing costs discussed in the Abe reference has absolutely nothing to do with the attachment of the semiconductor element 14 to the leadframe 10 through the use of the adhesive tape 12. Rather, the manufacturing cost reductions are achieved by the protrusion of the terminal portions 10a through the substrate mount surface of the resin material 18 and application of the solder layers 19 thereto which allows the terminal portions 10a to be used as connecting terminals.

Thus, it does not appear that one of ordinary skill in the art considering the Huang et al reference would be motivated to combine the teachings of the Abe reference thereto for purposes of modifying the package structure 300 to have portions of the first chip 304 attached to the first surfaces 328a of the leads 326. There is simply no teaching in the Abe reference regarding a correlation between the reduction in manufacturing costs argued by the Examiner and the attachment of the semiconductor element 14 to the leadframe 10. If one of ordinary skill in the art were to take the actual manufacturing cost reduction teachings of the Abe reference and apply them to the package structure 300 shown in Figure 7 of the Huang et al reference, such package structure 300 would be modified in a manner wherein the leads

326 could effectively be used as connecting terminals to eliminate the solder ball requirement of conventional ball-grid array semiconductor devices, the second surface 328b of each such lead 326 including a solder layer applied thereto to assist in use as such a connecting terminal. Thus, Applicant respectfully submits that it is only with a disfavored hindsight consideration of the teachings of the Huang et al and Abe references that the Examiner is able to support the hypothetical combination relied upon in the latest Office Action.

Even assuming, arguendo, that the hypothetical combination of the Huang et al and Abe references is not based on disfavored hindsight as argued above, Applicant respectfully submits that such combination still does not teach, suggest or show the relative orientations between the bond pads of the first semiconductor die and the leads as recited in each of amended independent Claims 1 and 19 as highlighted above. In this regard, there is clearly no teaching in the Huang et al reference regarding the orientation of the first bonding pads 308 of the first chip 304 between respective pairs of the leads 326. Indeed, a review of Figure 4 of the Huang et al reference and the corresponding passage of the specification thereof demonstrates that if the leads 326 were enlarged to extend beneath the first chip 304, many if not all of the bonding pads 308 of the first chip 304 would be completely or at least partially covered by the leads 326, as opposed to the bonding pads 308 being oriented between respective pairs of the leads 326. The Examiner's reliance upon Figures 1 and 7 of the Huang et al to support the rejections of Claims 10 and 25, respectively, appears to be misplaced since neither of these Figures even remotely depicts the spatial relationship between the bond pads and leads as recited in these claims and thus now recited in the amended versions of independent Claims 1 and 19. Since the Abe reference is also completely devoid of any teaching or suggestion regarding this spatial relationship, Applicant respectfully submits that it would clearly only be through the application of disfavored hindsight that the combined teachings of the Huang et al and Abe references could be used to satisfy the recitations in each of independent Claims 1 and 19 as amended. Thus, Applicant respectfully submits that independent Claims 1 and 19 as amended are in condition for

allowance, as are Claims 2-9, 11, and 20-24 as being dependent upon respective allowable base claims.

Conclusion

On the basis of the foregoing, Applicant respectfully submits that the stated grounds of rejection have been overcome, and that Claims 1-9, 11 and 19-24 are now in condition for allowance. An early Notice of Allowance is therefore respectfully requested.

If any additional fee is required, please charge Deposit Account Number 19-4330.

Respectfully submitted,

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